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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TRINH, MICHAEL MANH

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/020,407

Applicant(s)

MADGE ET AL.

Examiner

Michael Trinh

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-7 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 8-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Art Unit: 2822

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on February 12, 2003.

Claims 1-13 are pending, in which claims, 11-13 have been newly added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 11, 12, and 13 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 5, 6, and 7, respectively, in this present application. For example, since claim 11 depends on independent claim 1, by incorporating all limitations of independent claim 1 into dependent claim 11, the incorporated claim 11 is identical to that of independent claim 5 (similar discussions are to claims 12 and 13). This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thibeault ("On the Comparison of Iddq Testing" VLSI Test Symposium 1999, pp 143-150), and further of Sabade ("Improved wafer-level spatial analysis or Iddq limit setting", Test Conference 2001, pp 82-91).

Rejection and reasons in the last office action are repeated hereafter for convenience.

Thibeault discloses a method comprising the steps of: measuring quiescent current of chip to chip or wafer to wafer vectors (column 2, lines 22-29); calculating a difference between a

Art Unit: 2822

value of the selected parameter at a target location and that of an identical relative location with respect to the target location for each of the plurality of electronic circuits to generate a distribution of differences (col 3, lines 9-16); calculating an absolute value of the distribution of differences (Figure 1; col 3, line 38 through col u, line 4); and calculating an average of the absolute value of the distribution of differences to generate a representative value for the residual for the identical relative location (figure 5).

Thibeault fails to disclose the measuring of quiescent current in neighboring die or plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameters.

Sabade et al disclose measuring of quiescent current in neighboring die (page 83-page 84), plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter (Figs 4-5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Thibeault to measure the quiescent current of neighboring die as taught by Sabade et al in order to estimate the process gradient in local wafer regions. It also would have been obvious to plot the residual to determine a spatial correlation pattern in order to show the quiescent current projections on the XY plane of the wafer.

4. Claim 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thibeault ("On the Comparison of Iddq Testing" VLSI Test Symposium 1999, pp 143-150), and further of Sabade ("Improved wafer-level spatial analysis or Iddq limit setting", Test Conference 2001, pp 82-91).

Rejection and reasons in the last office action are repeated hereafter for convenience.

Thibeault discloses a method comprising the steps of: measuring quiescent current of chip to chip or wafer to wafer vectors (column 2, lines 22-29); calculating a difference between a value of the selected parameter at a target location and that of an identical relative location with respect to the target location for each of the plurality of electronic circuits to generate a distribution of differences (col 3, lines 9-16); calculating an absolute value of the distribution of differences (Figure 1; col 3, line 38 through col u, line 4); and calculating an average of the

Art Unit: 2822

absolute value of the distribution of differences to generate a representative value for the residual for the identical relative location (figure 5).

Thibeault fails to disclose the measuring of quiescent current in neighboring die or plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameters. Thibeault also fails to disclose the rejection of any of the plural integrated circuit die having a quiescent current value outside the expected value range.

Sabade et al disclose measuring of quiescent current in neighboring die (page 83-page 84), and plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter (Figs 4-5). Sabade et al also disclose the rejection of any of the plural integrated circuit die having a quiescent current value outside the expected value range (page 85, elimination of gross outliers).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Thibeault to measure the quiescent current of neighboring die as taught by Sabade et al in order to estimate the process gradient in local wafer regions. It also would have been obvious to plot the residual to determine a spatial correlation pattern in order to show the quiescent current projections on the XY plane of the wafer. Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to reject any of the plural integrated circuit die having a quiescent current value outside the expected value range as taught by Sabade in order to obtain a good estimate of fault free Iddq and to eliminate maverick lots.

Allowable Subject Matter

5. Claims 5-7 are allowed.
6. The following is a statement of reasons for the indication of allowable subject matter:

As objected to as being dependent upon a rejected base claim in the last office action, Applicant rewritten claims 5 and 6 in independent form including all of the limitations of the base claims 1 and any intervening claims. Accordingly, Claims 5 and 6 are allowed. Claim 7 is allowed as depending upon allowed base claim 6. The relied references of record including Thibeault and Sabade, alone or in combination, do not fairly disclose or make a prima facie

Art Unit: 2822

obvious case of the method for detecting variations in a spatially correlated parameter comprising all of process limitations as claimed, with the inclusion in claim 5 of performing a lot averaging for each wafer x-y coordinate so that a new set of best estimates is re-calculated for each x-y position, and with the inclusion in claim 6 that the common substrate comprises a plurality of common substrates wherein best estimates for a given x-y location are identical to those of a corresponding location on another of the plurality of common substrates.

Response to Arguments

7. Applicant's remarks filed on February 12, 2003 have been fully considered but they are not persuasive, and are also moot in view of the new ground(s) of rejection.

** Applicant remarks (at remark pages 5-6) that "...the pair of adjacent vector locations disclosed in Thibeault used to calculate differences is not equivalent to the claimed identical relative location...", wherein "each pair of location vectors considered in Thibeault may be represented as two adjacent locations (i) and (i-1). In contrast, the claimed identical relative location is independent of vector distance. An example of the claimed identical relative location is described in the specification...as (-5,10)...".

In response, this is noted and found unconvincing. Applicant appears to read into the claims the identical relative location, for example, as (-5,10), that is, 5 units in the negative X direction and 10 units in the positive Y direction. However, the claims do not recite any relative coordinates. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In *Re Self*, 213 USPQ 1,5 (CCPA 1982); In *Re Priest*, 199 USPQ 11,15 (CCPA 1978).

Thibeault calculates a difference between a quiescent current value at a target location (i) and that of an identical relative location (i-1) with respect to the target location (i), wherein there is no other relative location, for example, (i-2) or (i+1).

*** Applicant further remarked that "...because both relative coordinates (1,0) and (0,1) differ from the corresponding target location by only one unit in vector distance..., the relative coordinates (1,0) and (0,1) are clearly not identical...".

Art Unit: 2822

In response, this is noted and found unconvincing. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. Although the (1,0) and (0,1) relative coordinates are not identical, both relative coordinates (1,0) from one target location and relative coordinates (1,0) from a different target location are identical, wherein both relative coordinates (1,0) also differ from respective target locations by only one unit in vector distance. In any event, Thibeault calculated a difference between a quiescent current value at a target location (i) and that of an identical relative location (i-1) with respect to the target location (i), wherein there is no other relative locations, for example, (i-2) or (i+1). Noting claimed subject matter, not the specification, is the measure of invention.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs


Michael Trinh
Primary Examiner